Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte MARIUS ORLOWSKI,
KUO-TUNG CHANG, KEITH E. WITEK
and JON FITCH

_____

Appeal No. 1999-1637
Application 08/417,537

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ON BRIEF

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Before THOMAS, LALL, and GROSS, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board under 35 U.S.C. §134 from the examiner's non-final rejection in Paper No. 21 dated September 16, 1998. The appeal is proper since the claims have been twice rejected within this statutory provision. Of the pending claims 1-46 in the application, the examiner has allowed claims 9-17, 21-29 and 44-46

and has objected to claims 4, 7, 20, 32, 33 and 37-43. Thus, claims 1-3, 5, 6, 8, 18, 19, 30, 31 and 34-36 remain for our consideration on appeal.

Rep resentative claim 18 is reproduced below:

18. A semiconductor device comprising:

a substrate;

a first transistor overlying the substrate, the first transistor having a first current electrode underlying a channel region, and a select gate electrode laterally adjacent the channel region; and

a second transistor overlying the first transistor and being serially coupled to the first transistor, the second transistor having a second current electrode overlying the channel region wherein the first and second current electrodes are separated by the channel region, a floating gate electrode adjacent the channel region, and a control gate electrode laterally adjacent the floating gate electrode, wherein the second transistor is a floating gate storage transistor for storing a logic bit value and the first transistor is a select gate for selecting the second transistor.

The following references are relied on by the examiner:

Ono	5,402,371	Mar. 28, 1995 (filing date Oct. 7, 1993)
Wong	5,739,567	Apr. 14, 1998 (effective filing date Nov. 2, 1992)
Sugaya (Japanese Kokai)	61-256673	Nov. 14, 1986

Claims 18, 19, 30, 31, 34 and 35 stand rejected under 35 U.S.C. §102(e) as being anticipated by Wong. The examiner sites Figures 9 and 10 of this reference.

Claims 1-3, 5, 6, 8, 18, 19, 30 and 36 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Ono in view of Sugaya.

Rather than repeat the positions of the appellants and the examiner, reference is made to the briefs and the answer for the respective details thereof.

OPINION

Turning first to the rejection of the claims under 35 U.S.C. § 102, we sustain the rejection of claims 18, 30, 31, 34 and 35 as being anticipated by Wong, but reverse the rejection of claim 19. Wong appears to correspond to appellants' admitted prior art trench-based split gate devices as discussed at specificatioin page 2.

As to independent claims 18 and 30 rejected over Wong, appellants' common argument at pages 36, 37, 40 and 41 of the principal brief on appeal alleges that there is no select gate in Wong to meet the feature recited in these independent claims on appeal. The examiner addresses this argument at the bottom of page 4 of the answer by making reference to Figure 9 and observing that the select transistor 922 in Figure 9 has its own

channel region including channel length 923 and, more importantly, that the control gate 909 of the floating gate transistor 921 serves as the control gate for transistor 921 as well as the gate for the select transistor 922. We agree with the interpretation of Wong and such is buttressed by the discussion at column 8, lines 30-38, for example, of Wong.

As we read the discussion of the rejection under 35 U.S.C. § 102 at pages 5-8 of the reply brief, appellants appear to implicitly agree with the examiner's characterization with respect to Figure 9, but seem to complain of some element of surprise with respect to the examiner's reliance upon this figure. Again, this rejection was initially stated in Paper No. 21 on September 16, 1998. From this rejection appellants filed a Notice of Appeal on December 14, 1998 and their brief on December 21, 1998. No responsive argument or secondary amendment was supplied in response to the non final rejection in Paper No. 21 before appeal was taken. The examiner maintained the same position in the answer as to how he viewed the applicability of Figures 9 and 10 to the noted claims on appeal in the same manner done in the rejection in Paper No. 21. It appears to us that appellants have lost the opportunity to amend the claims on appeal to read over or distinguish the features taught and suggested in Figures 9 and 10 of Wong. We are not persuaded of any reason to invoke our powers within 37 CFR §1.196(c) as requested in the reply brief. Since the

examiner introduced the reliance upon Wong in Paper No. 21 as outlined earlier, appellants have consistently referred only to Figure 10 in their discussion and have not addressed any teaching value of Figure 9 as also relied upon by the examiner in the rejection. Moreover, even Figure 10E appears to present the same final structure of the method of making the various devices in Wong as is present in structural form in Figure 9A and Figure 9B anyway.

We agree with appellants' view expressed at page 37 of the principal brief on appeal that Wong does not teach the features recited in claim 19 on appeal. This claim requires that the channel region be a cylindrical region where the floating gate surrounds, in the form of a sidewall spacer, the cylindrical channel region. It appears to us that the opposite is true in Figure 9A and Figure B as well as the Figure 10E showings in Wong. Whereas the claimed floating gate is claimed to be on the outside of a cylindrical channel region in claim 19, these figures in Wong clearly show a floating gate region 905 surrounded by the channel region 903 comprising portions 903A and 903B.

We agree with the examiner's rejection of dependent claims 31, 34 and 35. The discussion of Figure 10 begins at the bottom portion of column 8 through the top of column 11 where Figure 10E is specifically discussed. However, in the intervening

columns it is taught that various well known fabrication techniques such as doping, implanting and diffusion as expressed in dependent claims 34 and 35 are utilized as well as etching to form the various regions comprising the various embodiments in Wong's whole patent. We are unpersuaded of appellants' position as to claim 31 that the claimed process forms a sidewall spacer as a floating gate over the entire select gate and that such is not done in Wong. There is no order recited in claims 31, 34 and 35 of the manner or the timing in which the various regions are formed, contrary to the apparent position taken by appellants as to these claims. In accordance with the examiner's views as to Figures 9A and 9B as well as Figure 10E, the claim 31 feature is met in that the floating gate does appear to be formed above the formation of the select gate within the channel region 903B/923 of the select transistor 922.

Lastly, we turn to the rejection of claims 1-3, 5, 6, 8, 18, 19, 30 and 36 as being obvious over the combined teachings and showings of Ono in view of Sugaya. We reverse this rejection.

Ono's Figure 1 shows a conventional sidewall-type flash EEPROM cell with three gates comprising two transistors for each cell, such as the cells depicted in Figure 3 of this reference. On the other hand, Sugaya is a single transistor device for the memory cells per

se where Figure 1 shows two cells connected together. In this reference there is no select transistor and therefore no select gate comparable to the second transistor of Ono's Figure 1, which includes the sidewall gate or select gate 18.

From our study of the examiner's position at pages 3-5 of the answer, the examiner proposes to modify Ono's prior art horizontal floating gate EEPROM memory cell arrangement in view of the vertically structured floating gate cell in Sugaya. However, the examiner's explanation of this combination does not propose any manner of a structural combination, only that it would have been obvious to fabricate Ono's device vertically as done in Sugaya rather than horizontally.

On the basis of the examiner's position as well as our study of both references, we conclude that the examiner has not established a prima facie case of obviousness within 35 U.S.C. § 103. Indeed, we have concluded that there appears to be no clear basis from the teachings and suggestions in both references as well as the examiner's reasoning as to how the artisan would have modified the two transistor memory cells of Ono which is based on a horizontal architectural approach in view of the vertical architectural approach of Sugaya. The combination appears to us to be problematic because the examiner's reasoning and the references do not account for any manner in which the second transistor

or a select transistor as in Ono would be fabricated in a vertical orientation and its placement with respect to the other elements shown, for example, in Sugaya's Figure 1. Thus, we are left without any clear guidance as to where the location would be of the select gate or sidewall gate 18 from Ono's Figure 1 in Sugaya's vertical architectural approach in his representative Figure 1.

In order for us to sustain the examiner's rejection under 35 U.S.C. § 103, we would need to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis of the rejections. In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968), reh'g denied, 390 U.S. 1000 (1968). This we decline to do. Thus, we can only but conclude that without more evidence, the references are not properly combinable within 35 U.S.C. § 103.

In considering the teachings and showings of Sugaya alone as applicable to independent claims 1, 5, 18, 30 and 36 within this rejection of those claims on appeal, we conclude that Sugaya alone does not teach or show the entirety of each of these respective independent claims. The only gates shown in representative Figure 1 of Sugaya are the floating gate 2 and the control gate 1. Since claim 1 recites a first vertically disposed gate that is a floating gate, this would correspond to floating gate 2 in Sugaya's Figure 1. However, this floating gate does not overlie the previously recited horizontally disposed gate electrode in claim 1 since the only other gate shown in Figure 1 of Sugaya

is the control gate 1. It may be fairly characterized as being located laterally adjacent to the floating gate 2.

The recitation of the floating gate overlying another gate is also recited in independent claim 5 on appeal. However, this claim also requires specifically that that gate be a select gate. Since Sugaya's invention does not include a select transistor and therefore a select gate for the dual memory cell arrangement in representative Figure 1, the overall structure of claim 5 on appeal can not be met by Sugaya alone. Claim 18 cannot be met for similar reasons. This claim also recites a first and second transistor, only one of which may be arguably met in any manner by the teachings and showings in Sugaya's Figure 1. Finally, independent claims 30 and 36 on appeal require the recitation of a select gate which is not taught or suggested in any manner in Sugaya as discussed earlier. Since we can not sustain any rejection of independent claims 1, 5, 18, 30 and 36 on the basis of Sugaya alone, the rejection of their respective dependent claims must also be reversed.

In closing, we have sustained the rejection of claims 18, 30, 31, 34 and 35 under 35 U.S.C. § 102, while reversing the rejection of dependent claim 19 on this statutory basis. We have also reversed the rejection of all claims on appeal under 35 U.S.C. § 103. Therefore, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

James D. Thomas Administrative Patent Judge	))))) BOARD OF PATENT
Parshotam S. Lall Administrative Patent Judge	)) APPEALS AND)) INTERFERENCES
Anita Pellman Gross Administrative Patent Judge	))

JDT/cam

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